I CLAIM:

1. A multiple-phase DC-DC converter, comprising:

an N-phase switching regulator which provides an output voltage V_{out} at an output terminal, each of said phases comprising:

an output inductor, and

a switching circuit which switches current to and from said output inductor in response to a respective control signal;

a control circuit which provides said N control signals to said N phases during a switching cycle which has a period T and a frequency *f1*, said control signals phase-shifted by T/N with respect to each other such that said phases are synchronously switched in a prescribed sequence, said phases providing respective phase currents which are summed together; and

at least one additional phase, each of said additional phases comprising a current generating circuit which provides a current I_{hp} in response to a control signal, said current I_{hp} having a switching frequency *f2* which is equal to or greater than *f1*, said current I_{hp} summed with said N phase currents to provide an output current I_{out} to a load connected to said output terminal, said current I_{hp} providing energy which improves the converter's response to load changes.

2. The DC-DC converter of claim 1, wherein said current generating circuit comprises:

a driver connected to receive said additional phase's control signal and to toggle an output in response,

an output inductor connected between said output terminal and a common node, and

a switching circuit connected to said common node and arranged to conduct current to and from said current generating circuit's output inductor in response to said driver output to provide said current I_{hp}.

3. The DC-DC converter of claim 2, wherein said current generating circuit further comprises a logic gate which receives said N control signals at respective inputs and provides said additional phase's control signal at an output such that the switching frequency *f2* of said additional phase's control signal is equal to N*f1.

4. The DC-DC converter of claim 2, wherein said switching circuit comprises:

a first transistor connected between a supply voltage and said common node, and

a second transistor connected between said common node and ground,

said current generating circuit arranged such that said second transistor is turned off and said first transistor is turned on and conducts current between said supply voltage and said current generating circuit's output inductor when said driver output is in a first state, and such that said first transistor is turned off and said second transistor is turned on and conducts current between said current generating circuit's output inductor and ground when said driver output is in a second state.

5. The DC-DC converter of claim 4, further comprising a capacitor connected between said common node and said output inductor such that current I_{hp} is substantially an AC current.

6. The DC-DC converter of claim 5, wherein each of said additional phases has a higher switching frequency and

a smaller output inductor than do said N phases such that said additional phase's output current I_{hp} responds faster to load changes than do said N phase currents, and said N phases exhibit a higher efficiency than said additional phases.

7. The DC-DC converter of claim 1, wherein said control signals are pulse-width modulated (PWM).

8. The DC-DC converter of claim 1, wherein said control circuit is arranged to inhibit the operation of said N phases when said load is below a predetermined level, such that I_{out} is entirely provided by said at least one additional phase.

9. A multiple-phase DC-DC converter, comprising:

an N-phase switching regulator which provides an output voltage V_{out} at an output terminal, each of said phases comprising:

an output inductor, and

a switching circuit which conducts current to and from said output inductor in response to a respective control signal;

a control circuit which provides said N control signals to said N phases during a switching cycle which has a period T and a frequency *f*, said control signals phase-shifted by T/N with respect to each other such that said phases are synchronously switched in a prescribed sequence, said phases providing respective phase currents which are summed together; and

at least one additional phase, each of said additional phases comprising:

a logic gate which receives said N control signals at respective inputs and combines them into a single control signal which has a switching frequency equal

to N*f,

a driver connected to receive said single control signal and to toggle an output when any of said N control signals are provided to their respective phases,

an output inductor connected between said output terminal and a common node, and

a switching circuit connected to said common node and arranged to conduct current to and from said output inductor in response to said driver output to provide a current I_{hp} having a switching frequency equal to N*f, said current I_{hp} summed with said N phase currents to provide an output current I_{out} to a load connected to said output terminal, said current I_{hp} providing energy which improves the converter's response to load changes.

10. The DC-DC converter of claim 9, wherein said switching circuit comprises:

a first transistor connected between a supply voltage and said common node, and

a second transistor connected between said common node and ground,

said at least one additional phase arranged such that said second transistor is turned off and said first transistor is turned on and conducts current between said supply voltage and said additional phase's output inductor when said driver output is in a first state, and such that said first transistor is turned off and said second transistor is turned on and conducts current between said common node and said additional phase's output inductor when said driver output is in a second state.

11. The DC-DC converter of claim 10, further comprising a capacitor connected between said common node and said output inductor such that current I_{hp} is substantially an AC current.

12. The DC-DC converter of claim 11, wherein each of said additional phases has a higher switching frequency and a smaller output inductor than do said N phases such that said additional phase's output current I_{hp} responds faster to load changes than do said N phase currents, and said N phases exhibit a higher efficiency than said additional phases.

13. A multiple-phase DC-DC converter, comprising:

an N-phase switching regulator which provides an output voltage V_{out} at an output terminal, each of said phases comprising:

an output inductor, and

a switching circuit which conducts current to and from said output inductor in response to a respective pulse-width modulated (PWM) control signal;

a control circuit which provides said N control signals to said N phases during a switching cycle which has a period T and a frequency *f*, said control signals phase-shifted by T/N with respect to each other such that said phases are synchronously switched in a prescribed sequence, said phases providing respective phase currents which are summed together to provide an output current I_{out} to a load connected to said output terminal, the duty cycles of said N PWM control signals varying with said load, and

at least one additional phase arranged to reduce I_{out} by a current I_{hp} when the duty cycles of all of said control signals are approximately zero due to a load release, to reduce V_{out} overshoot that might otherwise occur in response to said load release.

14. The DC-DC converter of claim 13, wherein said control circuit further provides a clock signal Fclk which is pulsed at the start of each of said N control signals'

switching periods such that Fclk has a frequency N*f, each of said additional phases comprising:

a logic gate which receives said N control signals and combines them into a single control signal Fpwm which has a switching frequency equal to N*f when the duty cycles of said N control signals is non-zero,

a reset-dominate flip-flop connected to receive said control signal Fpwm at its reset input and said clock signal Fclk at its set input such that said flip-flop's output is reset whenever a non-zero Fpwm control signal is received and is set whenever Fpwm is zero when Fclk is received, and

an output current reduction circuit coupled to said flip-flop output and arranged to conduct said current I_{hp} when said flip-flop output is set.

15. The DC-DC converter of claim 14, wherein each of said output current reduction circuits comprises:

an output inductor connected between said output terminal and a common node and which conducts current I_{hp}, and

a switching circuit connected between said common node and a ground terminal and arranged such that said switching circuit conducts current from said output inductor to ground when said flip-flop output is set.

16. The DC-DC converter of claim 15, wherein said N phases are arranged such that the maximum slew rate S_{off} at which said N phases can reduce I_{out} in response to a load release is given by:

$S_{off}=-ND(VCC/L)$,

where VCC is said N-phase switching regulator's input voltage, D is given by V_{out}/VCC, and L is the inductance of the active phase's output inductor,

the output current I_{hp} of each additional phase

having a slew rate S_{hp} which increases the overall slew rate S_{ft} at which said DC-DC converter can reduce I_{out} in response to a load release, S_{ft} given by:

$S_{ft} = S_{off} - S_{hp} = -[(N/L) + (1/L_{ph})] * D * VCC$,

where L_{ph} is the inductance of said output current reduction circuit's output inductor.

17. The DC-DC converter of claim 15, wherein said output current reduction circuit further comprises:

an RC network connected between said common node and a supply voltage, and

a diode connected between said common node and said supply voltage,

such that the current in said output current reduction circuit's output inductor is reset to zero when said flip-flop is reset.

18. The DC-DC converter of claim 13, wherein said multiple-phase DC-DC converter is a buck converter having an input voltage VCC, said buck converter arranged such that $ND<1$, where D is given by V_{out}/VCC.

19. A multiple-phase DC-DC converter, comprising:

an N-phase switching regulator which receives an input voltage VCC, provides an output voltage V_{out} at an output terminal, and is arranged such that $ND<1$, where D is given by V_{out}/VCC, each of said phases comprising:

an output inductor, and

a switching circuit which conducts current to and from said output inductor in response to a respective pulse-width modulated (PWM) control signal;

a control circuit which provides said N control signals to said N phases during a switching cycle which has a period T and a frequency *f*, said control signals phase-shifted by T/N with respect to each other such that said

phases are synchronously switched in a prescribed sequence, said phases providing respective phase currents which are summed together to provide an output current I_{out} to a load connected to said output terminal, the duty cycles of said N PWM control signals varying with said load, said control circuit further providing a clock signal Fclk which is pulsed at the start of each of said N control signals' switching periods such that Fclk has a frequency N*f, and

at least one additional phase arranged to reduce I_{out} by a current I_{hp} when the duty cycles of all of said control signals are approximately zero due to a load release, to reduce V_{out} overshoot that might otherwise occur in response to said load release, each of said additional phases comprising:

a logic gate which receives said N control signals and combines them into a single control signal Fpwm which has a switching frequency equal to N*f when the duty cycles of said N control signals is non-zero,

a reset-dominate flip-flop connected to receive said control signal Fpwm at its reset input and said clock signal Fclk at its set input such that said flip-flop's output is reset whenever a non-zero Fpwm control signal is received and is set whenever Fpwm is zero when Fclk is received, and

an output current reduction circuit coupled to said flip-flop output and arranged to conduct said current I_{hp} when said flip-flop output is set.

20. The DC-DC converter of claim 19, wherein said output current reduction circuit comprises:

an RC network connected between a common node and a supply voltage,

a diode connected between said common node and said supply voltage,

an output inductor connected between said output

terminal and said common node and which conducts current I_{hp}, and

a switching circuit connected between said common node and a ground terminal and arranged to conduct current from said output current reduction circuit's output inductor to ground when said flip-flop output is set and such that the current in said output current reduction circuit's output inductor is reset to zero when said flip-flop is reset.

21. The DC-DC converter of claim 20, wherein said N phases are arranged such that the maximum slew rate S_{off} at which said N phases can reduce I_{out} in response to a load release is given by:

$S_{off}=-ND(VCC/L)$,

where VCC is said N-phase switching regulator's input voltage, D is given by V_{out}/VCC, and L is the inductance of the active phase's output inductor,

the output current I_{hp} of each additional phase having a slew rate S_{hp} which increases the overall slew rate S_{ft} at which said DC-DC converter can reduce I_{out} in response to a load release, S_{ft} given by:

$S_{ft} = S_{off}-S_{hp} = -[(N/L)+(1/L_{ph})]*D*VCC$,

where L_{ph} is the inductance of said output current reduction circuit's output inductor.